## CLAIMS

*What is claimed is:*

1. A method of forming an antifuse on a semiconductor substrate, the method comprising:

providing a partially formed semiconductor device having a substrate;

implanting nitrogen into a first portion of the substrate of an unmasked portion of the partially formed semiconductor device;

growing a dielectric oxide layer on the nitrided first portion of the substrate using a wet oxidation process; and

depositing a gate material directly on the dielectric oxide layer, wherein the gate material comprises one terminal of the antifuse.

2. The method of forming an antifuse as recited in claim 1, wherein the nitrogen is implanted using a dose in the range from about $5 \times 10^{13}$ atoms/cm$^2$ to $1 \times 10^{15}$ atoms/cm$^2$ of nitrogen.

3. The method of forming an antifuse as recited in claim 1, wherein the nitrogen is implanted using an energy in the range from about 5 to 50 Kev.

4. The method of forming an antifuse as recited in claim 1, wherein the nitrogen implant dose is about $4 \times 10^{14}$ atoms/cm$^2$ implanted at an energy of about 25 Kev.

5. The method of forming an antifuse as recited in claim 1, wherein the wet oxidation process takes place at a temperature in the range from 800 to 900 degrees C.

6. The method of forming an antifuse as recited in claim 1, wherein a sacrificial oxide layer is first grown on the substrate and the nitrogen is implanted within 200-600 Angstroms of the interface between the sacrificial oxide and the substrate.

7. The method of forming an antifuse as recited in claim 1, wherein the thickness of the grown dielectric oxide layer is in the range from 30 to 40 Angstroms.

8. The method of forming an antifuse as recited in claim 1, wherein the thickness of the grown dielectric oxide layer is in the range from 40 to 60 Angstroms.

9. The method of forming an antifuse as recited in claim 1, further comprising implanting a second portion of the substrate with nitrogen and oxidizing the second portion in a wet environment at the same time as the dielectric oxide layer to form a second gate oxide having a thickness different than the dielectric oxide layer.

10. The method of forming an antifuse as recited in claim 9, wherein the dose of the nitrogen in the second portion is different than the dose in the first portion.

11. A method of determining the programmed state of an antifuse formed on a semiconductor substrate, the method comprising:

implanting nitrogen into a first portion of the substrate;

growing an oxide dielectric layer on the nitrided first portion using a wet oxidation process;

forming a patterned gate on the oxide dielectric layer to form the gate node of the antifuse;

forming at least one active region in the substrate, wherein the at least one active region is coupled to a ground voltage to form a ground node and arranged with the oxide dielectric and patterned gate to form the antifuse having the gate node and the ground node;

coupling the gate node to a voltage supply; and

determining the programmed state of the antifuse by sensing the voltage or current at the gate node.

12. The method of determining the programmed state of an antifuse as recited in claim 11, wherein the gate node is switchably coupled to the voltage supply.

13. The method of determining the programmed state of an antifuse as recited in claim 11, wherein a transistor is connected in series between the voltage supply and the gate node and a switchable connection between the voltage supply and gate node is controlled by a voltage input provided to the gate of the transistor.

14. The method of determining the programmed state of an antifuse as recited in claim 11, wherein sensing the voltage or current at the gate node includes electrically connecting the gate node to a sense amplifier.

15. The method of determining the programmed state of an antifuse as recited in claim 11, wherein the antifuse is programmable by the application of a second voltage between the gate node and the ground node and wherein the second voltage is higher than the supply voltage.

16. A system for monitoring the programmed state of an antifuse formed on a semiconductor substrate, the system comprising:

an antifuse including a gate oxide formed by implanting nitrogen into a first portion of the substrate and growing the gate oxide on the nitrided first portion using a wet oxidation process; a gate formed on the gate oxide, and a doped active region formed adjacent to a channel region of the substrate directly underneath the gate, wherein the antifuse gate forms an antifuse gate node and the doped active region is connected to a grounded voltage to form a ground node; and

a switching transistor having one of its source and drain regions coupled to the antifuse gate node and the other of the source and drain regions coupled to a voltage supply for switchably applying the supply voltage to the antifuse, wherein the system is configured to access the antifuse in order to determine its programmed state by providing a predetermined voltage to the gate of the switching transistor.

17. The system as recited in claim 16, further comprising a sense amp coupled to the gate node for sensing the voltage or current at the gate node.

18. The system as recited in claim 16, wherein the antifuse is programmable by the application of a voltage higher than the supply voltage to the antifuse gate node.